

Goal

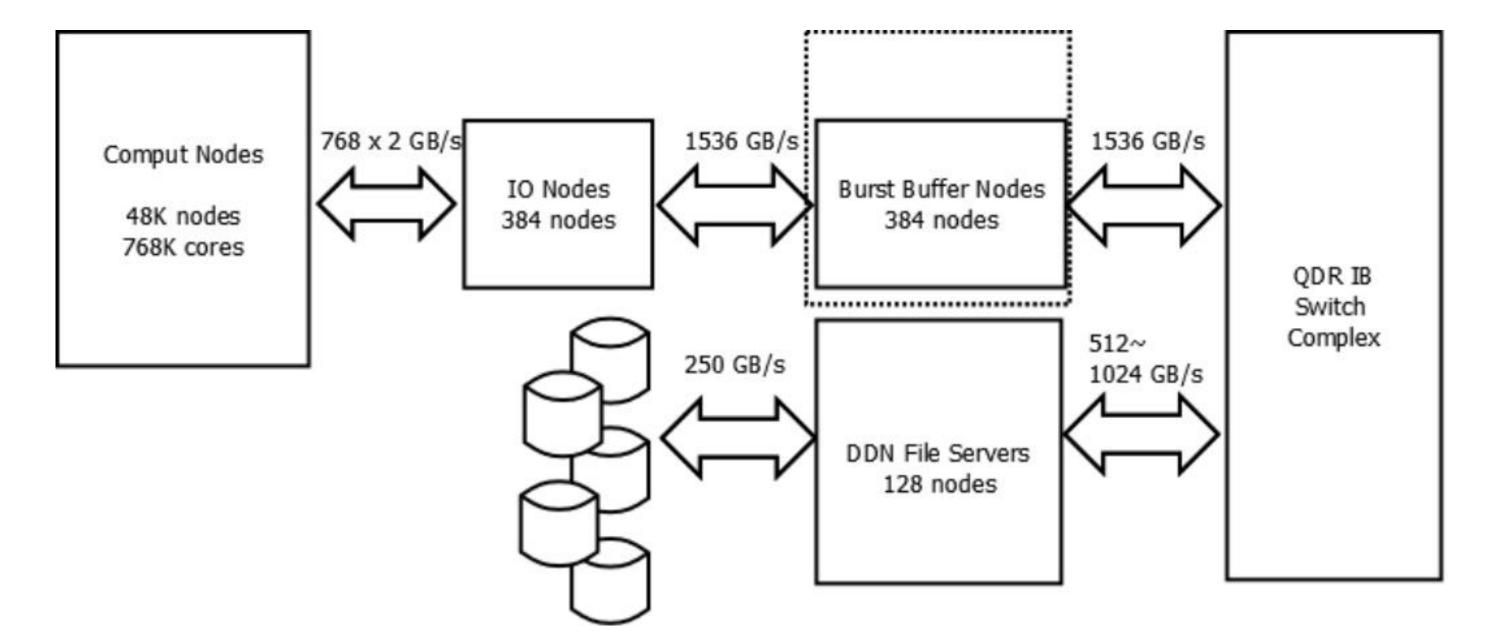
In this poster, we simulated the burst buffer storage architecture on an IBM BlueGene/Q supercomputer (with a 5D Torus network interconnect) using the CODES/ROSS simulation framework to study the potential I/O performance improvement with burst buffers. These results are a stepping stone towards studying this new storage architecture on future dragon-fly network based supercomputers, including resource management covering both storage and job scheduling.

Introduction

Burst buffer architecture has been proposed to handle bursty I/O patterns in HPC We have implemented a write protocol simulating the file write procedure on Mira as systems[1]. Burst buffers are high-throughput, low-capacity storage devices that act as a staging area or a write-behind cache for HPC storage systems. The approach we Figure 2. follow to incorporate burst buffers is to place these buffers on I/O nodes that connect to the external storage system and to manage these buffers as part of the Figure 2 Mira simulated file write protocol I/O forwarding services. If burst buffers are sufficiently large and fast, they can absorb I/O bursts [2]. Meanwhile, burst buffer layer can provide some distributed **Compute Node** file systems [7] more opportunities to improve data locality which is crucial for APP 6. fwrite_done() 1. fwrite() application performance [8]. pvfsd

We have implemented our simulation using CODES (Co-Design of Multilayer Exascale Storage Architectures)[3] and ROSS (Rensselaer Optimistic Simulation System)[4] simulation frameworks. ROSS is a parallel discrete event simulator which uses time warp protocols[5] to simulate discrete events in parallel.

Figure 1 Modeling Blue Gene/Q (Mira)



We measure the performance of our simulation for I/O operations of in Intrepid and Mira at ALCF and compare the performance of the burst buffer architecture to architecture without burst buffers through simulations. Figure 1 shows the Blue Gene/Q (Mira) modeling details

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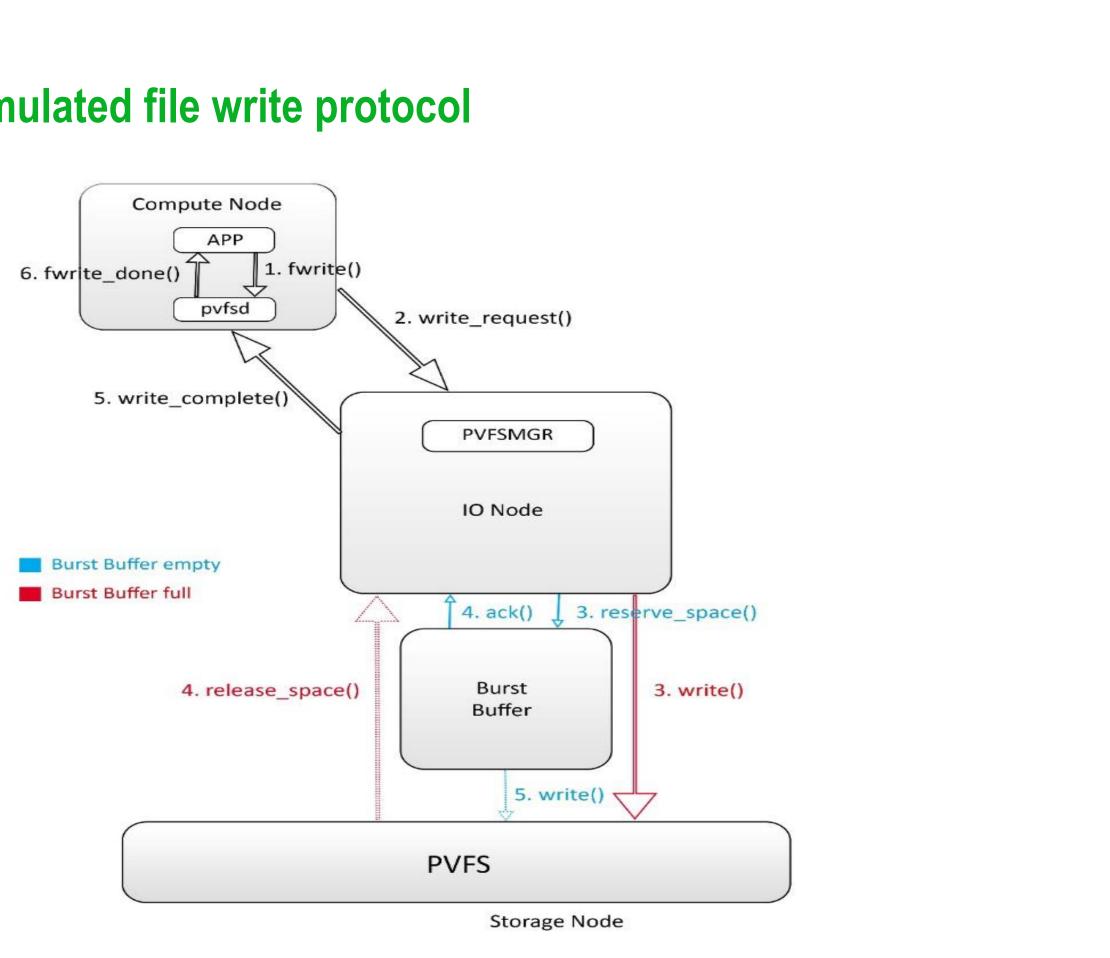
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Simulating the Burst Buffer Storage Architecture on an IBM BlueGene/Q Supercomputer

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Implementation

Figure 1 is our modeling details of Mira. Compute nodes(CN) are located in a 5D torus network. There are 16 computing cores on each CN. One midplane contains 512 CNs in 4 × 4 × 4 × 4 × 2 structure. One rack contains 2 midplanes and Mira has 48 racks which sums up to 49,152 CNs, 786,432 cores. The bandwidth of the torus link is 2GB/s in both directions. There are 384 IO nodes(ION) connected to the torus network through specialized compute nodes called "bridge nodes". The CN/ION ratio in our simulation is 128: 1. The bandwidth of each interconnection link between ION and DDN file system server is 4GB/s, which sums up to 1536 GB/s. There are 128 DDN file servers connected to disk arrays with total bandwidth of 250GB/s [6].



Results

We conducted several sets of experiments with configurations of Intrepid and Mira. The largest scale is up to 131,072 compute processes. Figure 3 (left) shows the aggregated write throughput with burst buffer enabled or not. Figure 3 (right) shows the per IO node throughput with burst buffer enabled or not.

Conclusion

From current results, we can conclude that:

- At the scale we run our experiments (upto 131,072 cores), burst buffers can scale very well in current Blue Gene/P and Blue Gene/Q storage architecture.
- The interconnection network between IO nodes and burst buffer nodes will be the bottleneck of full utilization of buffer buffers.
- bringing storage closer to the compute nodes can have a significant positive impact on performance

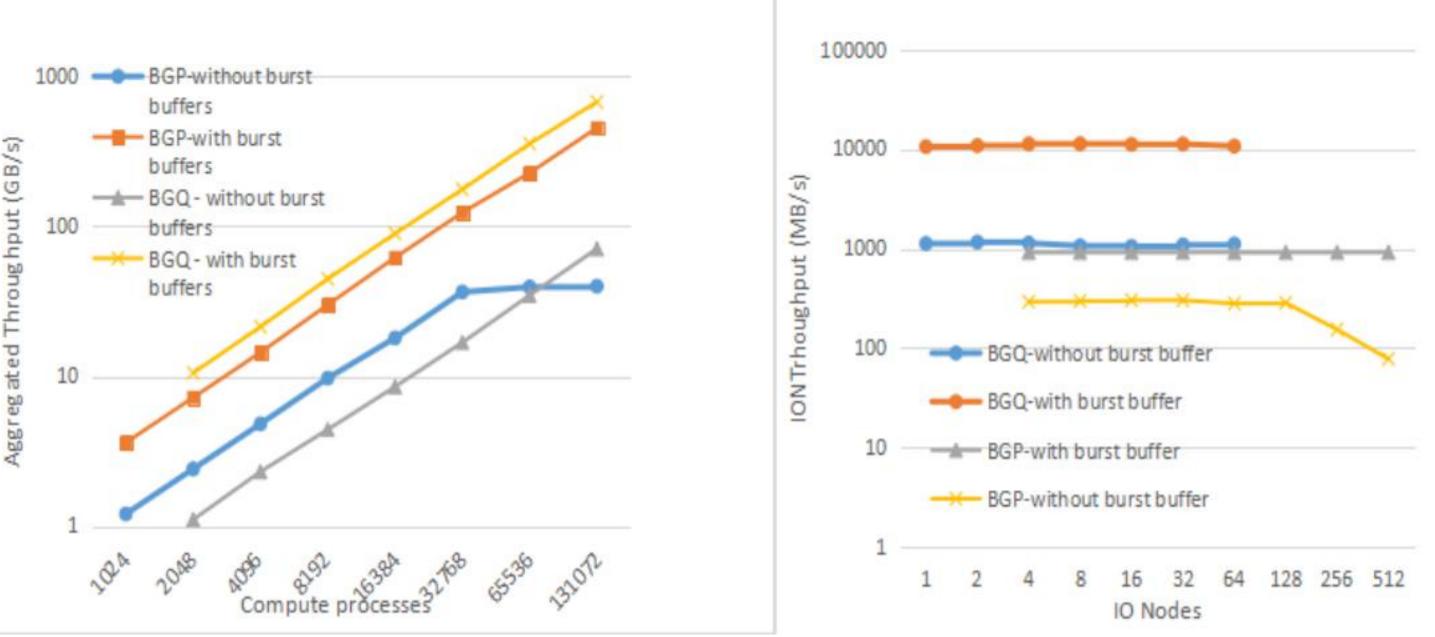


Figure 3 Simulation results

Related work

- Burst Buffer simulation on Intrepid
- Parallel File System simulators
- CODES network modeling framework
- ROSS masive parallel discrete-event simulator

Future work

Simulating supercomputers with dragon-fly network topologies, to study the effectiveness of the burst buffer architecture. We also plan to explore real application IO traces. Furthermore, we will also study burst buffer aware job scheduling, where data movement between burst buffers and persistent storage, and among the burst buffer resources, can be minimized

Acknowledgments

We would like to thank Jonathan Jenkins at ANL for his help in CODES. We also would like to thank Ning Liu for his experience from previous work.

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